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Modeling of planar carbon nanotube field effect transistor and three dimensional simulation of current-voltage characteristics

Dinh Sy Hien[1], **Nguyen Thi Luong**[1], **Thi Tran Anh Tuan** [1] **and Dinh Viet Nga**[1]

[1] HCM University of Natural Sciences, 227 Nguyen Van Cu Street, 5 District, Ho Chi Minh City, Vietnam

E-mail: vietnga704@yahoo.com

Abstract. We provide a CNTFET model with planar geometry. Planar CNTFETs constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. We explore the possibilities of using non-equilibrium Green function method to get I-V characteristics for CNTFETs. This simulator also includes a graphic user interface (GUI) of Matlab that enables parameter entry, calculation control, intuitive display of calculation results, and in-situ data analysis methods. In this paper, we review the capabilities of simulator, and give examples of typical CNTFET 3D simulations. The I-V characteristics of CNTFET are also presented.

Keywords: Planar CNTFET, GUI, NEGF, simulation of I-V characteristic of CNTFET.

1. Introduction

The carbon nanotube field-effect transistor (CNTFET) is a promising candidate for future electron devices. Rapid progress in the field has recently made it possible to fabricate CNTFET based circuits, such as logic gates, static memory cells, and ring oscillators.

This three-terminal device consists of a semiconducting nanotube bridging two contacts (source and drain) and acting as a carrier channel, which is turned on or off electrostatically via the third contact (gate). Presently, there are various groups pursuing the fabrication of such devices in several variations, achieving increasing success in pushing performance limits, while encountering myriad problems, as expected for any technology in its infancy. Although progress in CNTFETs has been rapid, there are still many issues to address.

In this work, we summarize experimental works on planar CNTFETs and introduce a CNTFET model with planar geometry. We also review the capabilities of the simulator, summarize the theoretical approach and experimental results, and give examples of typical planar CNTFET's 3D simulations (current-voltage characteristics which are functions of parameters such as the length of CNTFET, the gate thickness and temperature). The obtained I-V characteristics of the CNTFET are also presented by analytical equations.

2. Simulation results

2.1. Planar CNTFET geometry

We now provide a brief description of typical CNTFET geometries, which are grouped in two major categories, planar and coaxial. A CNTFET, whether planar or coaxial, relies on similar principles, while being governed by additional phenomena such as 1D density of states (DOS) and ballistic transport.

Planar CNTFETs constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The nanotube and the metallic source-drain contacts are arranged on an insulating substrate, with either the nanotube being draped over the pre-patterned contacts, or with the contacts being patterned over the nanotube. In the latter case, the nanotubes are usually dispersed in a solution and transferred to a substrate containing pre-arranged electrodes; transistors are formed by trial and error. Manipulation of an individual nanotube has also been achieved by using the tip of an atomic force microscope (AFM) to nudge it around the substrate; due to its strong, covalent bonds, this is possible to do without damaging the molecule. In the case where the electrodes are placed over the tube, manipulation of the CNT is not required and alignment markers, pre-arranged on the substrate, allow accurate positioning of the contacts once the nanotube is located via examination by a scanning tunneling microscope (STM). The gate electrode is almost always on the back side of the insulating substrate, or alternatively is patterned on top of an oxide-covered nanotube.

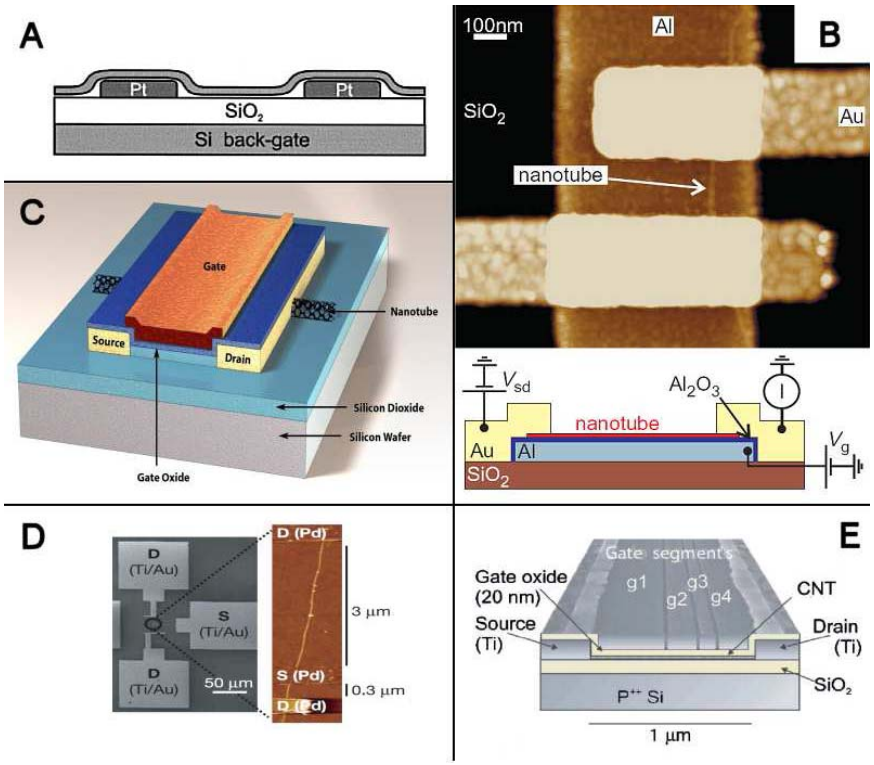

Figure 1. Examples of planar CNTFETs: (A) Ref. [1], (B) Ref. [2], (C) Ref. [3], (D) Ref. [4], and (E) Ref. [5].

The first CNTFET devices were reported in 1998, and involved the simplest possible fabrication. They consisted of highly-doped Si back gates, coated with thick SiO_2, and patterned source-drain metal contacts, either using Au or Pt, as shown in figure 1A [1]. Experimentations with different metals such as Ti, Ni, Al, and Pd have been carried out by several groups, primarily to manipulate the

work function difference between the end contacts and the nanotube. Subsequent work also produced a device that replaced the back gate with an electrode placed over the substrate, perpendicular to the source and drain contacts, as illustrated in figure 1B [2]. Here, the nanotube was separated from this gate electrode by a thin insulating layer of Al_2O_3, with the source-drain electrode strips placed over the tube ends. Recent theoretical studies comparing the interfaces between different bulk metals and metallic nanotubes, studying both end- and side-contacted tubes, concluded that Ti contacts yield superior conductance over their Au and Al counterpart's contact resistance. Figure 1C shows a further improvement in CNTFETs through the placement of the gate electrode over the semiconducting nanotube, thus improving the channel electrostatics via the thin gate oxide [3]. Moreover, the Ti source-drain metallization in this device form titanium carbide abrupt junctions with the nanotube, yielding increased conductance. Another attempt to obtain better gate electrostatics involved materials with high dielectric constants, such as zirconia (ZrO_2) and hafnia (HfO_2), being used as gate insulators. Figure 1D illustrates a device built with Pd source-drain contacts in order to exploit the sensitivity of this material's work function to hydrogen [4]. A multi-gate device, as shown in figure 1E, has recently been reported, whereby parallel top gates are used to independently control the electrostatics of different sections of the channel, thus facilitating a study of the transport characteristics of the nanotube channel [5]. Most recently, a device with excellent DC characteristics was fabricated with Pd end contacts, Al gate, and hafnia for the insulator. The coaxial geometry maximizes the capacitive coupling between the gate electrode and the nanotube surface, thereby inducing more channel charge at a given bias than other geometries. This improved coupling is desirable in mitigating the short-channel effects that plague technologies like CMOS as they downsize device features. It is also of importance to low-voltage applications, a dominating trend in the semiconductor industry and to allow, potentially, for easier integration with modern implementations of existing technologies such as CMOS. Besides the wraparound gate, special attention must also be paid to the geometry of the end contacts, since these play a role in determining the dimensions of the Schottky barriers that are present in the channel near the device ends and have a direct effect on current modulation. We hereinafter deal specifically with the planar geometry of the CNTFET.

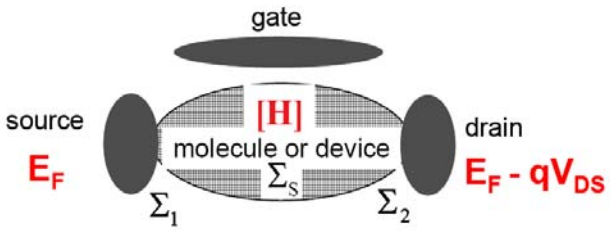

Figure 2. The generic transistor with a molecule or device channel connected to the source and drain contacts. The source-drain current is modulated by a third electrode, the gate. The quantities in the NEGF calculation are also shown.

2.2. Review of the NEGF formalism

A carbon nanotube can be viewed as a rolled-up sheet of graphene with a diameter typically between one and two nanometers. The nanotube can be either metallic or semiconducting, depending on how it is rolled up from the graphene sheet (i.e. depending on its chirality). Semiconducting nanotubes are suitable for transistors. In order to correctly treat carbon nanotube transistors, strong quantum confinement around the tube circumferential direction, quantum tunneling through Schottky barriers at the metal nanotube contacts, and quantum tunneling and reflection at barriers in nanotube channel need to be considered. The non-equilibrium Green's function (NEGF) formalism, which solves Schrödinger equation under non-equilibrium conditions and can treat coupling to contacts and dissipative scattering process, provides a sound basis for quantum device simulations. The NEGF simulation approach has demonstrated its usefulness for simulating nanoscale transistors from conventional Si MOSFETs, MOSFETs with novel channel materials, to CNTFETs [6], and molecular transistors [7]. In this section, we give brief summary of the NEGF simulation procedure. For a more thorough description of the technique, one can refer to work [8]. Figure 2 shows a generic transistor

and defines some terms for the NEGF simulation. The first step is to identify a suitable basis set and Hamiltonian matrix for an isolated channel. The self-consistent potential, which is a part of the Hamiltonian matrix, is included in this step. The second step is to compute the self-energy matrices, Σ_1, Σ_2 and Σ_S, which describe how the ballistic channel couples to the source-drain contacts and to the scattering process. For simplicity, only ballistic transport is treated in this work. After identifying the Hamiltonian matrix and the self-energies, the third step is to compute the retarded Green's function,

$$\mathbf{G}(E) = [(E + i0+)\mathbf{I} - \mathbf{H} - \Sigma_1 - \Sigma_2]^{-1} \quad (1)$$

The fourth step is to determine the physical quantities of interest from the Green's function. In the ballistic limit, states within the device can be divided into two parts: 1) states filled by carriers from the source according to the source Fermi level, and 2) states filled by the drain according to the drain Fermi level. Within the device, the source (drain) local-density-of-states (LDOS) is $\mathbf{D}_{S(D)} = \mathbf{G}\Gamma_{S(D)}\mathbf{G}^{+}$, where $\Gamma_{S(D)} = i(\Sigma_{1(2)} - \Sigma^{+}_{1(2)})$ is the energy level broadening due to the source (drain) contact. The charge density within the device is computed by integrating the LDOS, weighted by the appropriate Fermi level over energy. The charge contributed by the source contact is

$$Q_S(z) = (-e)\int_{E_N}^{+\infty} D_S(E,z) f(E - E_{FS}) dE + e\int_{-\infty}^{E_N} D_S(E,z)\{1 - f(E - E_{FS})\} dE \,, \quad (2)$$

where e is the electronic charge, and E_N is the charge neutrality level. The total charge is

$$Q(z) = Q_S(z) + Q_D(z) = (-e)\int_{-\infty}^{+\infty} dE.\mathrm{sgn}[E - E_N(z)]\{D_S(E,z) f(\mathrm{sgn}[E - E_N(z)](E - E_{FS})) + D_D(E,z) f(\mathrm{sgn}[E - E_N(z)](E - E_{FD}))\} \,, \quad (3)$$

where sgn (E) is the sign function, and $E_{FS,D}$ is the source (drain) Fermi level. For a self-consistent solution, the NEGF transport equation is solved with iteratively the Poisson equation until self-consistency is achieved after which the source-drain current is computed from:

$$I = \frac{4e}{h}\int T(E)[f_S(E) - f_D(E)] dE \,, \quad (4)$$

where T(E) = Trace ($G_1 G^{+}_2$) is the source-drain transmission and the extra factor of two comes from the valley degeneracy in the carbon nanotube energy band structure. The computationally expensive part of the NEGF simulation is finding the retarded Green's function, according to equation (1), which requires the inversion of a matrix for each energy grid point. The straightforward way is to explicitly invert the matrix, whose size is the size of the basis set. This, however, is impractical for an atomistic simulation of a nanotube transistor. In the ballistic limit, the problem is simplified because only a few columns of the Greens's function are needed. Still, reducing the size of the Hamiltonian matrix and developing computationally efficient approaches are of great importance for an atomistic simulation.

2.3. Main screen of planar CNTFET

Purpose of the project was to make a user-friendly simulator that provides as much control as possible over every aspect of the simulation. Consequently, graphic user interface (GUI) development in Matlab was a major part of the program. Here we present an overview of the most important GUI features.

The main screen shown in figure 3 is the central location where one can control the simulation programme. From the main screen, one can quickly enter simulation parameters with a minimum of typing. Clicking the left mouse pointer on each item of the main screen to enter the parameters such as types of source-drain materials (Au, Pt, Pd); types of gate materials (Al_2O_3 (k = 5), HfO_2 (k = 20), ZrO_2 (k = 26), TiO_2 (k = 65), $SiTiO_3$ (k = 175)); length of CNT (nm); temperature (K); the gate thickness (nm); colours (blue, green, pink, yellow, black); voltage V_g (V); V_d (V). Clicking the right mouse pointer on the item which is used to calculate the current voltage characteristics in 2D (plot I_d-V_{ds} or plot I_d-V_{gs}), reset used to clear current data or in 3D (plot I_d-V_{ds}-T, plot I_d-V_{ds}-L and plot

I_d-V_{ds}-t_{ox}). During calculation, symbol "running" will be appeared. Source-drain material (Au), Gate material (Al_2O_3, k = 3), Colour (red) are default settings. Simulations in 2D take less time than in 3D. Thanks to simulations in 3D, one can get more detail of tendency and effects of parameters such as temperature, the length of CNT, the gate thickness on I-V characteristics.

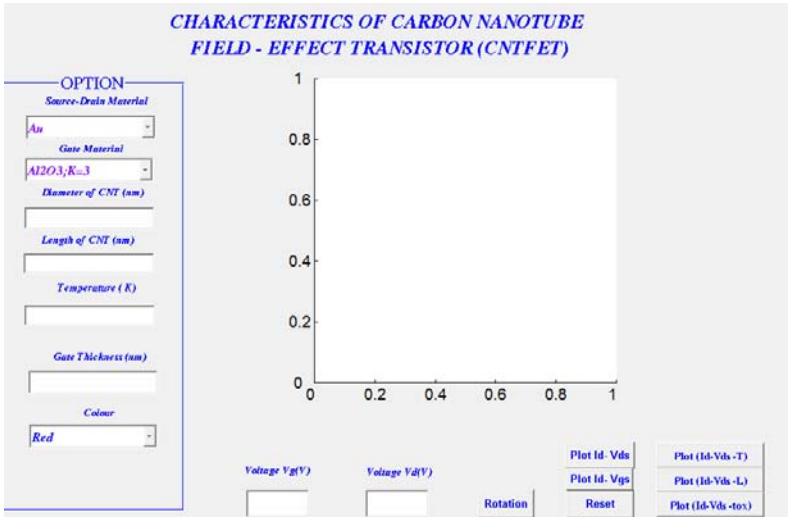

Figure 3. The main screen of simulation program of planar CNTFET. Source-drain material (Au), Gate material (Al_2O_3, k = 3), Colour (red) are default settings.

2.4. Simulations of current-voltage characteristics of planar CNTFET

The drain I-V characteristics in 2D are shown in figure 4. The saturation current at V_{GS} = 0.5 V is around 6 μA, which is not inconsistent with values emerging from recent experimental work [9].

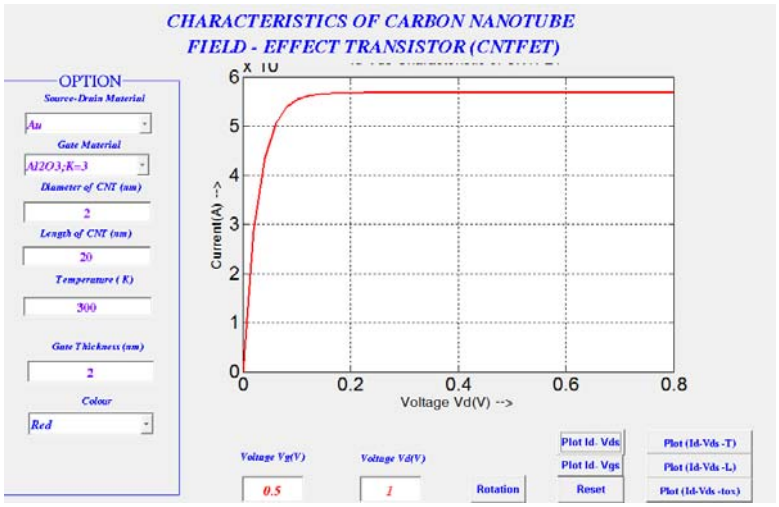

Figure 4. Drain current-voltage characteristics of planar CNTFET.

The drain I-V characteristics in 3D are shown in figure 5. The parameters used in 3D simulation are drain current-voltage characteristics and temperature. Drain I-V characteristics exhibited dependence

of saturation drain current on temperature. When CNTFET is cooled, drain saturation currents were lightly decreased.

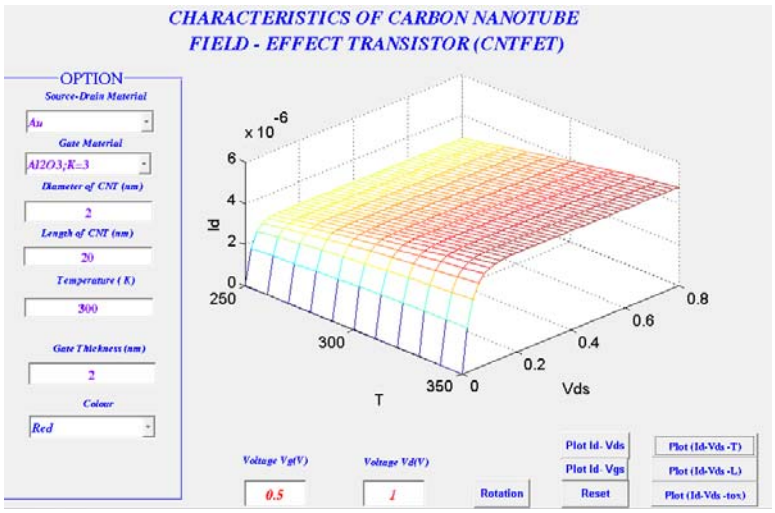

Figure 5. Drain current-voltage characteristics in 3D. When CNTFET is cooled, its saturation drain currents lightly decrease.

Drain current-voltage characteristics in 3D exhibited dependence of saturation currents on CNTFET length, L are shown in figure 6. Tendency of saturation currents is decreased, when CNTFET length is increased.

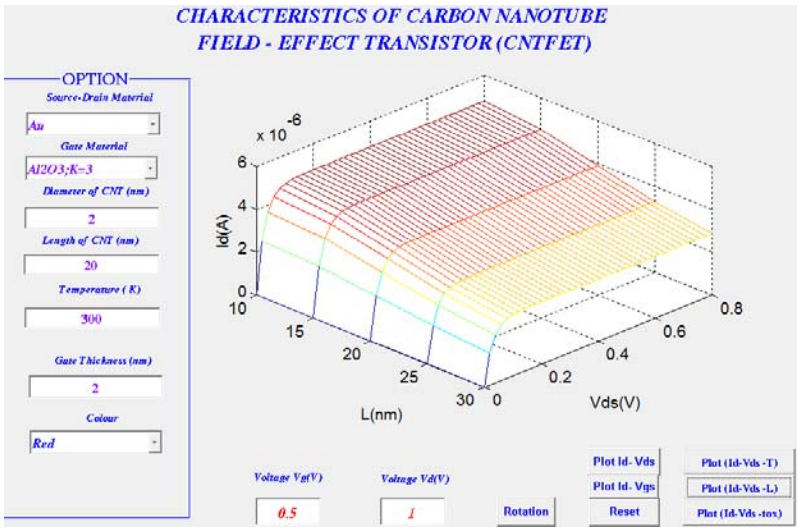

Figure 6. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on CNTFET length.

Drain current-voltage characteristics in 3D exhibited dependence of saturation current on the gate thickness of CNTFET, t_{ox} are shown in figure 7.

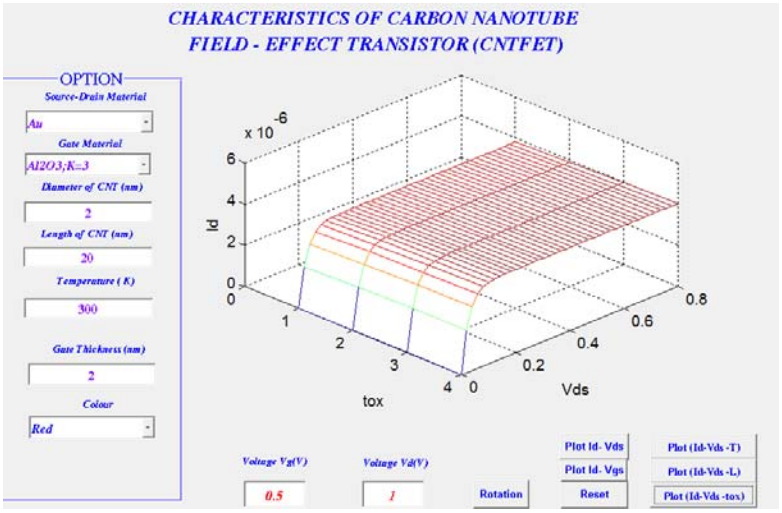

Figure 7. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on the gate thickness of CNTFET.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of CNTFET can be described as follows:

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] \quad (5)$$

or

$$I_d = K_n\left[2(V_{gs} - V_T)V_{ds} - V_{ds}^2\right] , \quad (6)$$

where K_n is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is mobility of carriers, C_{ox} is gate capacitance.

We can also obtain saturation current of CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written:

$$I_{d(sat)} = K_n(V_{gs} - V_T)^2 . \quad (7)$$

3. Conclusions

A planar model for CNTFET has been reported, which is specially intended for 3D simulations of drain current-voltage characteristics. The proposed model has been verified and a good agreement with recent experimental data [9] is found. A set of 3D simulations is then successfully performed for different parameters of materials, the length, the gate thickness of CNTFET, and temperature. The tendency and effects of these parameters on I-V characteristics have been predicted. Analytical equations of drain current-voltage curve have been also presented.

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